

This cross-sectional view shows a semiconductor device with two gate structures. The substrate 301 is divided into regions 305a and 305b by a central region 401. A base layer 302 is formed on the substrate. Above the base layer, there are three horizontal layers: 303, 306, and 307. Gate structures 304 and 308 are formed on the top surface, each consisting of a vertical sidewall 309 and a top layer 308. The regions 305a and 305b are defined by the gate structures and the base layer.

Fig. 2(a)

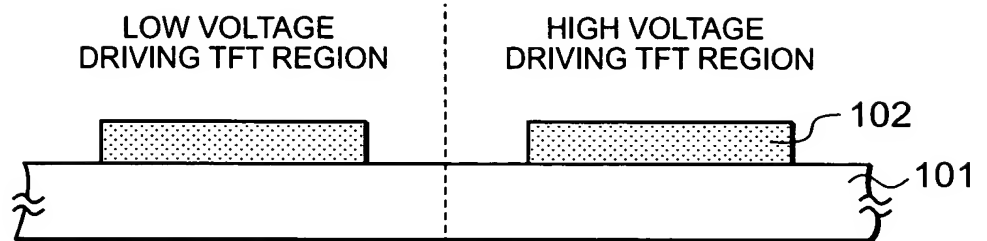


Fig. 2(b)

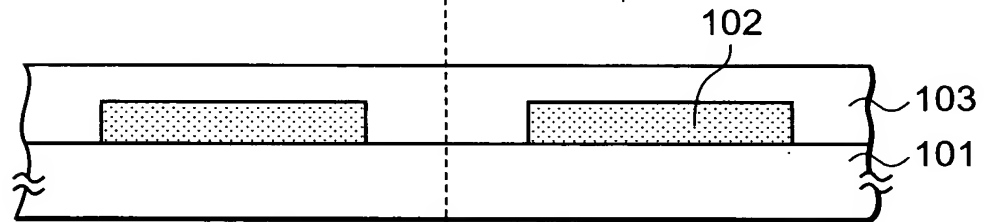


Fig. 2(c)

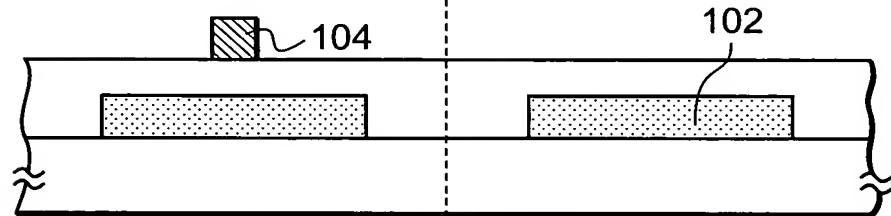


Fig. 2(d)

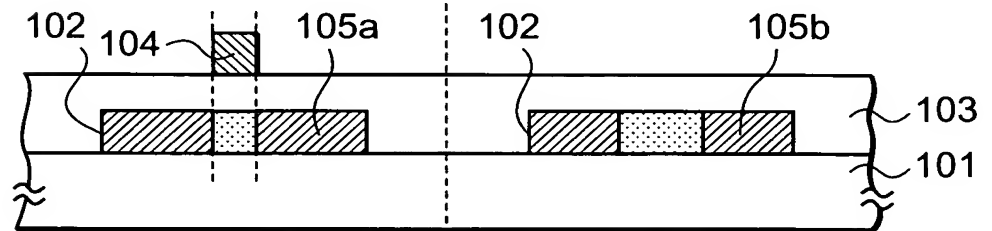


Fig. 3(a)

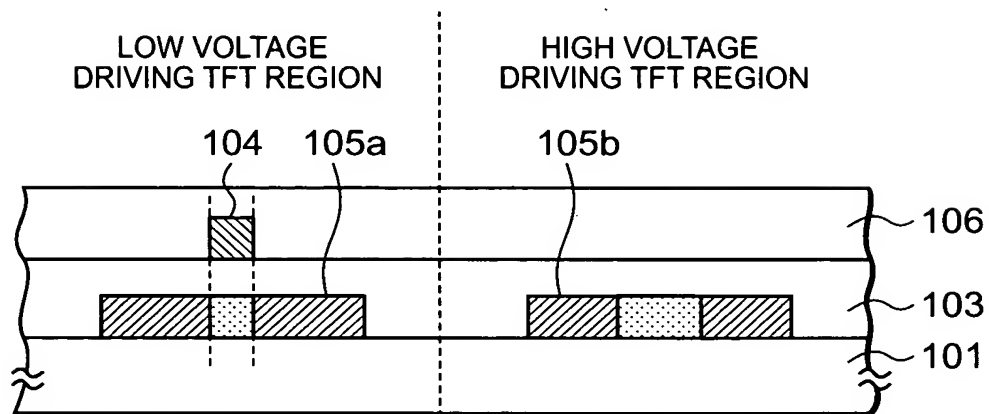


Fig. 3(b)

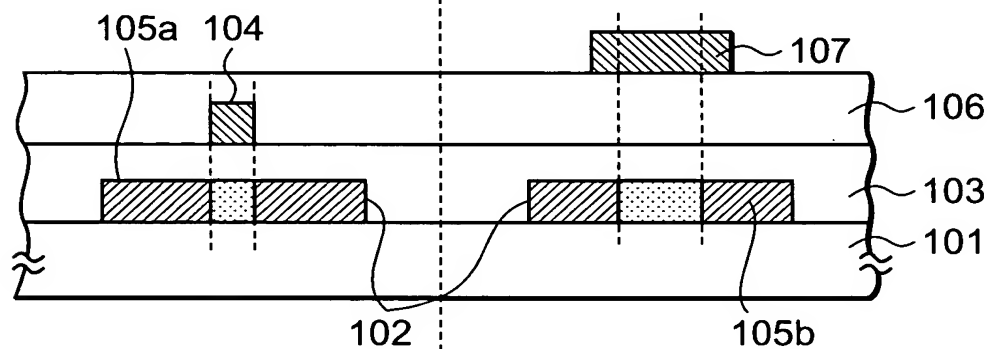


Fig. 3(c)

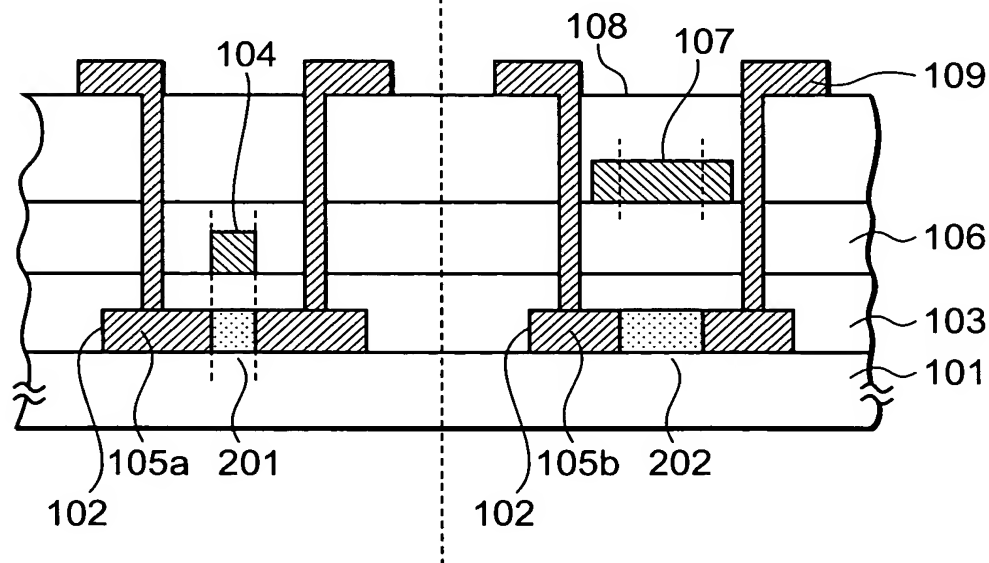


Fig. 4(a)

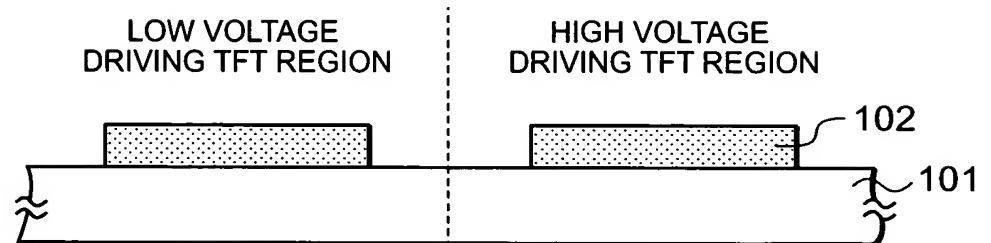


Fig. 4(b)

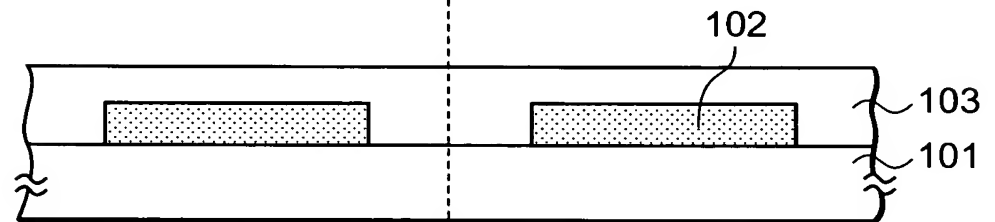


Fig. 4(c)

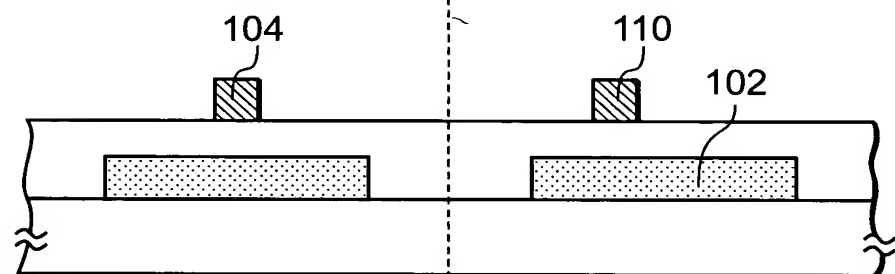


Fig. 4(d)

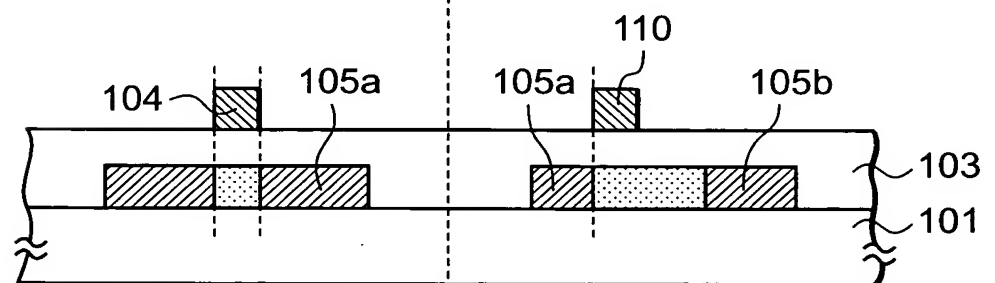


Fig. 5(a)

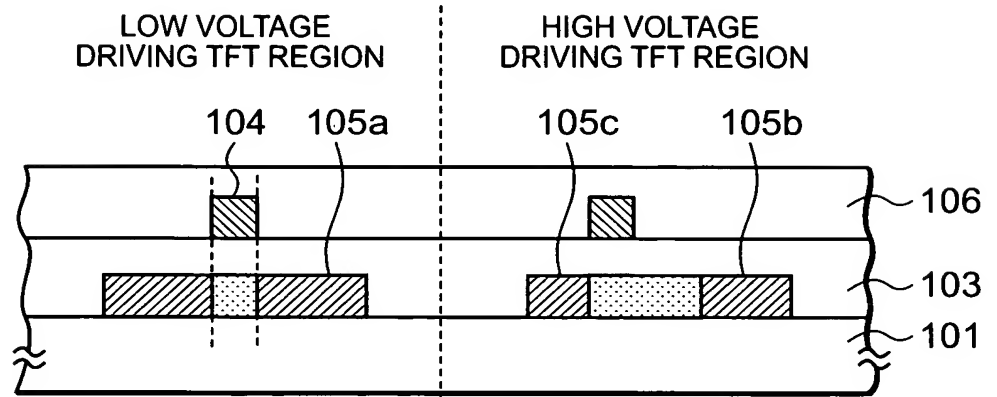


Fig. 5(b)

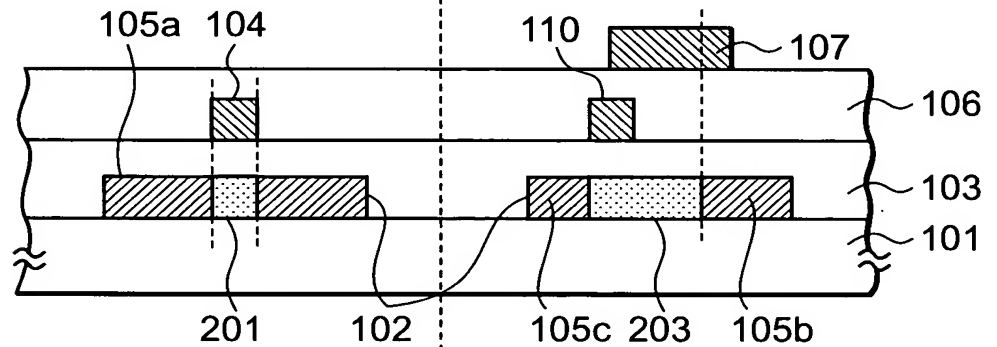


Fig. 5(c)

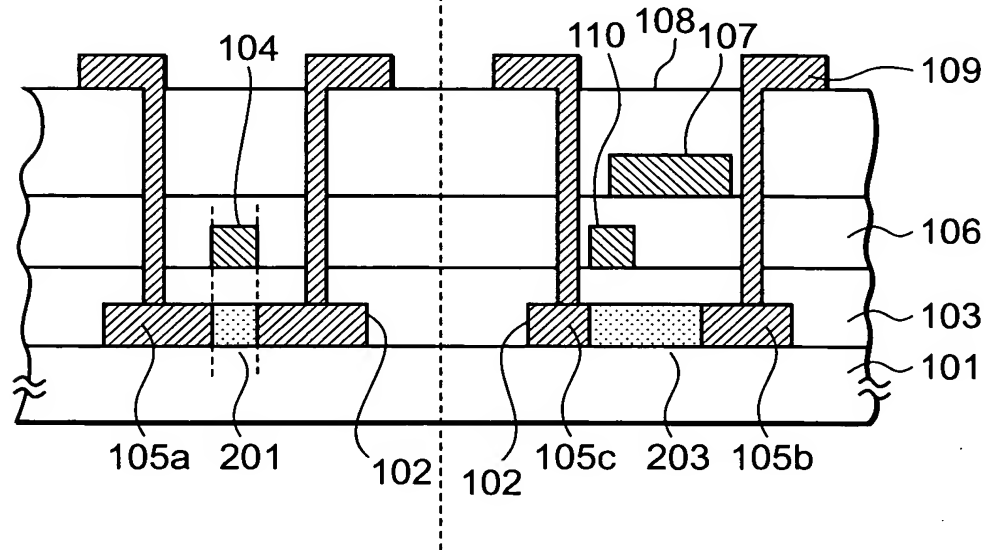


Fig. 6

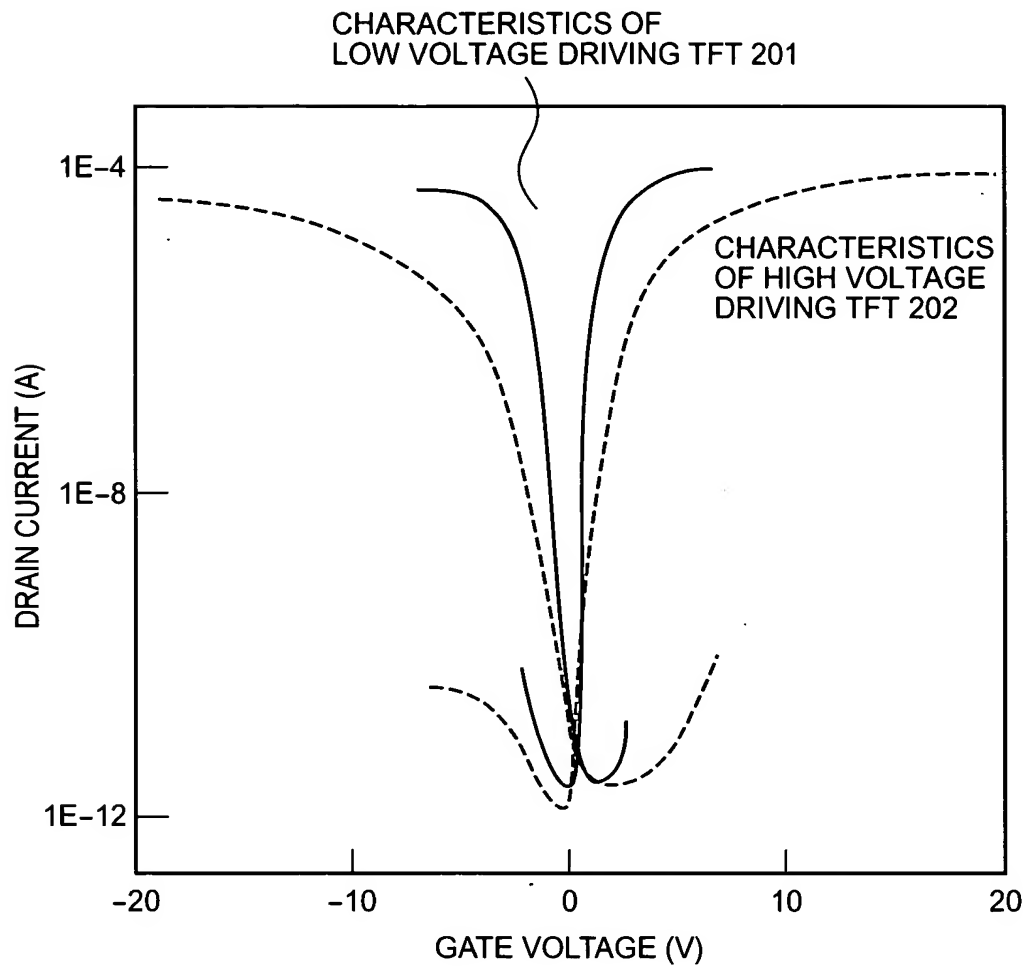


Fig. 7

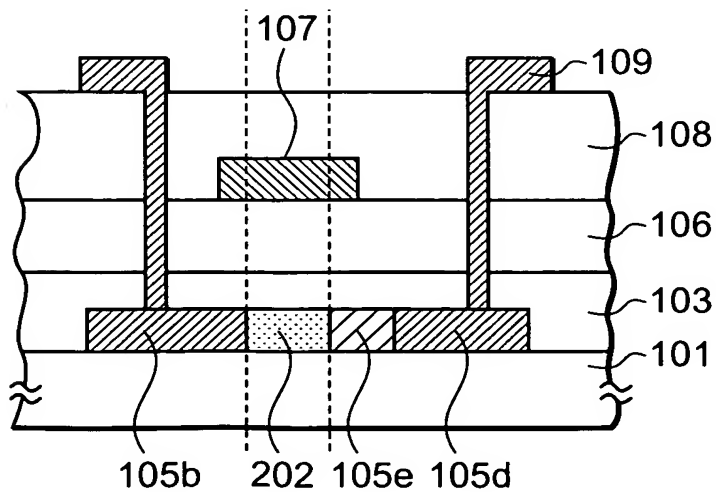


Fig. 8

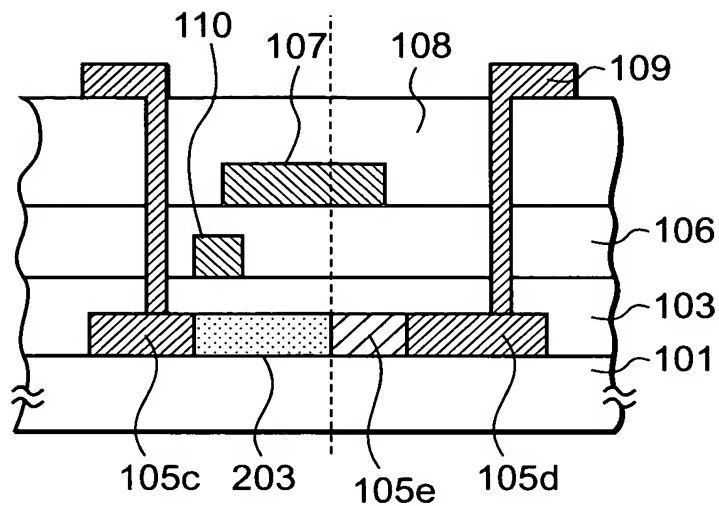


Fig. 9

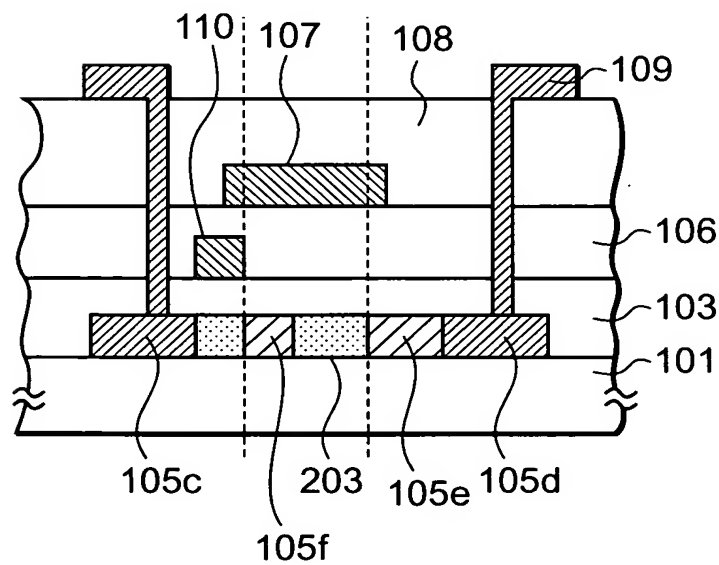


Fig. 10

